4 MUX 32CH Scanning Matrix Mini LED Driver

1. Features

- **Supply Voltage**
  - VDD 9~16V
- **32 High-Precision Current Sinks**
  - 40mA max. current per channel,
  - Adjustable range from 2.5mA to peak current
  - Independent 13-bit PWM duty cycle and 11-bit DC dimming control
- **Support 12-bit Global DC Dimming**
- **Build in Scan Line Driven**
  - MUX=4
  - Embedded high-side PMOS
- **Frequency multiplying support for VSYNC**
- **Feedback loop to optimize system power efficiency**
- **Channel grouping and delay for avoiding input current overshoot**
- **Slew rate control for MUX switches & current sink to optimize EMI performance**
- **40Hz ~ 0.5KHz VSYNC**
- **SPI Interface**
  - Max Speed 16MHz
  - Daisy chain and parallel structure capable
- **Protection:**
  - LED Open Detection by each zone
  - LED Short Detection by each zone
  - Thermal shutdown
  - Fault event will be indicated by INTB pin (open-drain)
- **WQFN-64L 7.0mm*7.0mm*0.75mm package**

2. Description

The HY88001 is a 128 zones passive matrix LED driver with independent channel control, designed for driving locally dimmed displays. The device supports 4 low-resistance high-side switches and 32 low-side current sinks that can deliver up to 40mA of continuous current per channel. The driver has 13-bit PWM duty cycle and 11-bit current control of each low-side LED current sink. An extra global 12-bit current control for all of channels provides a simple dimming control method.

Each current sink can be individually controlled through the SPI interface, but also has the capability to be controlled with a single value over the global brightness control register.

Programmable MUX phase shift and MUX gap offer a largest flexibility to synchronize LCD display frame.

A digital enhanced DC/DC feedback function is regulating any external SMPS to the best suitable output voltage needs of the LED strings to minimize power dissipation.

Full protections are included, including build-in LED open/short detection for each channel and device thermal shutdown.

3. Application

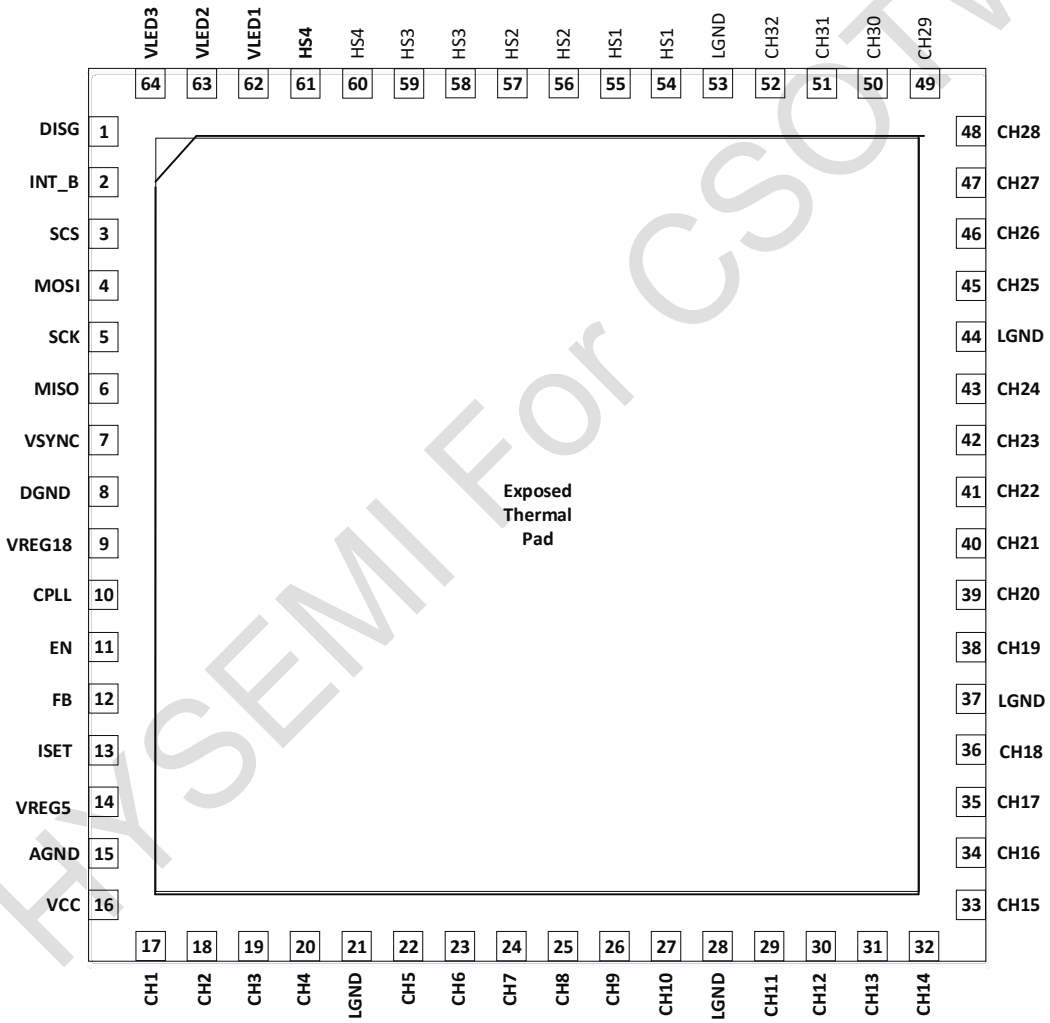
- **Control Panel Illumination**
- **Local Dimming LED Backlight Drivers**

Table of Contents

4. Ordering Information

Part Number	Package
HY88001	QFN7.0x7.0-64L

5. Package Outline



6. Pin Description

Pin Name	No.	Type	Description
VLED	3	Power	Input pin for high-side switches
VCC	1		Power supply
VREG5	1		Internal voltage regulator 5V output
VREG18	1		Internal voltage regulator 1.8V output
HS1 ~ HS4	8	Analog	High-side PMOS switch output for LED group 1 ~ 4
CH1 ~ CH32	32	Analog	Current channel 1 ~ 32
FB	1	Analog	The voltage on the pin "Outx" is monitored to adjust the power supply output voltage
EN	1	Input	Activate device, high active
SDI	1	Input	Master output, Slave input
SDO	1	Output	Master input, Slave output
SCLK	1	Input	SPI serial clock
SCS	1	Input	Chip select, high active
VSYNC	1	Input	Come from TCON, frame data update control Synchronization signal to LCD panel data display High active
INT_B	1	Output	Interrupt. LED Open/Short fault or thermal shutdown indicator. Open-drain
CPLL	1	Output	Loop filter for PLL
ISET	1	Output	LED channel current setting
DISG	1	Ground	MUX discharge ground
AGND	1		Analog ground
DGND	1		Digital ground for control logic
LGND	5		LED-driver ground

7. Feature Description

7.1. Power Supply (VLED)

It supplies power for LED matrix array and it passed through internal high side PMOS with Ron=0.14 ohm. Connect a ceramic capacitor (CVLED) to the VLED pin for stable of LED anode voltage. If the CVLED is not enough, it might be unstable.

7.2. Power Supply (VDD)

5.0V (VREG5) is generated from VCC after CEN=High. The VCC pin has a UVLO function and chip starts operation while VCC ≥ UVLO_up and stops operation after VCC ≤ UVLO_down. Connect a ceramic capacitor (CVCC) to the VCC pin for stable. The recommended value is 0.1μF. If the CVCC is not connected, it might occur unstability e.g. oscillation.

7.3. Internal Regulators & Compensation Pins

7.3.1. VREG5

“LDO 12V->5V” block generates 5.0V from VCC after CEN=High and outputs 5.0V to the VREG5 pin. This 5V voltage supplies is mainly the power source to internal analog circuit blocks. A reference voltage (VREF) comes from this voltage as well. It cannot supply power to external parts from VREG5 pin. The VREG5 pin has UVLO function. Connect a ceramic capacitor (CVREG5) to the VREG5 pin for phase margin. The recommended value is 2.2μF.

7.3.2. VREG18

LDO 5V->1.8V” block generates 1.8V from internal 5V power source. It also outputs 1.8V to the VREG18 pin. The 1.8V power source supplies to internal digital circuit. It has no driving cpability to supply external parts from VREG18 pin. An UVLO function monitors this voltage as well. Connect a ceramic capacitor (C_{VREG18}) to this pin for phase margin. The recommended value is 2.2μF. If the C_{VREG18} is not connected, it might be oscillation.

7.3.3. LDO 5V->3.3V

LDO 5V->3.3V” block generates 3.3V for all of the I/O pin operation. ANX54128 supports either 3.3V or 1.8V I/O capability to offer system’s flexibility on MCU selection. This 3.3V voltage is only for I/O interface purpose and no output to external pin.

7.3.4. LED Anode Control

- ***High-Side PMOS***

HY88001 integrates 4 high-side PMOS to minimize system dimension. These MOS components can sustain up to 36V external supply and carry maximum continuous 1.28A current passed through on each MOS. The typical Ron for each device is around 0.14ohm.
In order to reduce EMI interference on the edge of MUX turn on, 16 steps slew rate control with 100ns/step is available in HY88001.

- ***Dis-Charge Control***

In order to have a better non-overlap control between MUX switch, a programmable constant sink current path from HSn, n=1~4, to ground has been integrated with each high-side PMOS.
There are four levels of sink current to dis-charge the capacitance stored on HSn terminal. The corresponding faling speeds are fastest, fast, slow and slowest.

- ***MUX Delay Feature***

HY88001 offers maximum 1 frame delay from Vsync to first MUX activation with 13-Bit resolution.

7.3.5. LED Cathode Control

- ***Constant Current Driver***

Total 32 independent control current drivers serves four high-side PMOS paths to accomplish multiplexing structure. Each current driver has maximum 40mA capability with an appropriate external precise resistor to configure. Each current driver equips 11-bit DC current resolution and 13-bit PWM dimming resolution.

- ***PWM Dimming Control***

HY88001 supports 13-Bit PWM dimming control for individual LED zone.

- ***Local DC Dimming Control***

HY88001 supports 11-bit DC dimming control for individual LED zone.

- ***Global DC Dimming Control***

A 12-Bit DC dimming control can be applied to all of LED zone at the same time.

7.3.6. Feedback Control Mechanism

CHn, n=1~32, voltage is controlled by FB terminal. If minimum CHn voltage is less than head room voltage, It sinks current from FB terminal and VLED level will raise up. If minimum LEDCHn voltage is more than head room voltage and close to it, the feedback control loop is near to a stable state.

7.3.7. Protection

There are four protection behaviors in the HY88001 to make sure system operation with normally and safely

- ***LED Open Detection***

This detection mode is for individual LED zone. The detection threshold can be programmed by Open_thres[1:0] register. The values are 0.05V, 0.1V, 0.15V and 0.2V. The detail information about Open detection mechanism can refer to Timing Sequence section.

- ***LED Short Detection***

This detection mode is for individual LED zone. The detection threshold can be programmed by Short_thres[1:0] register. The values are 3V, 5V, 7V and 9V. The detail information about Short detection mechanism can refer to Timing Sequence section.

- ***UVLO***

There are three UVLO detections on VCC, VREG5 and VREG1.8 rail to make sure chip's normal operation.

- ***Thermal Shutdown***

Once the junction temperature is over 145℃, chip will be shut down. While the temperature go back to under 115℃, system will restart to operate again.

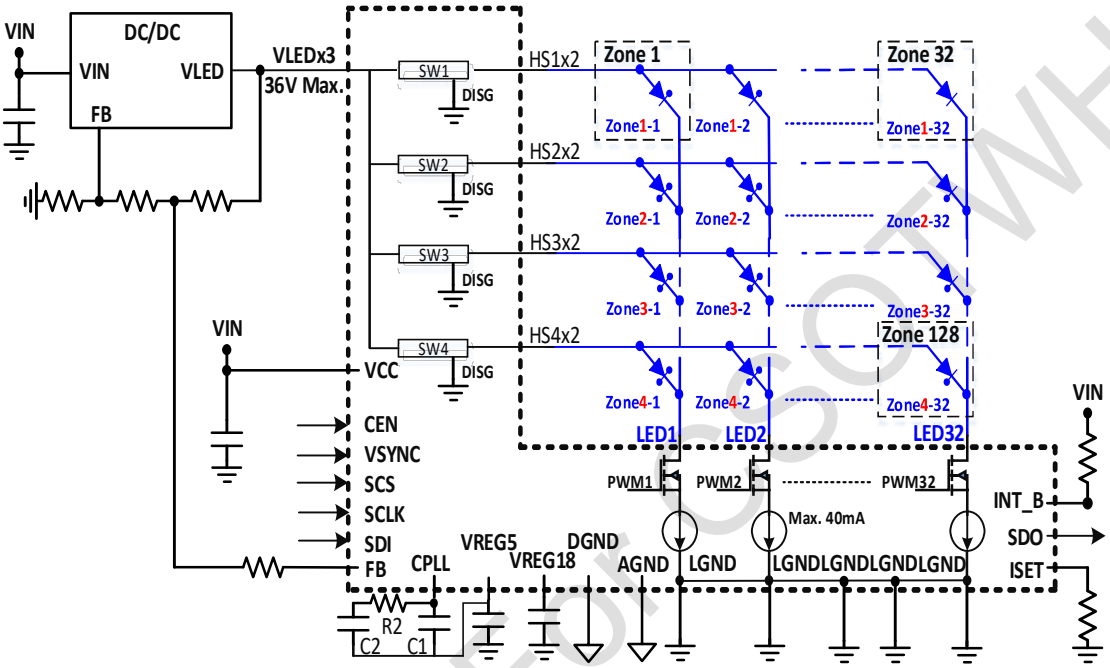
7.3.8. I/O Pins

All of the digital I/O pins are supported 3.3V or 1.8V signaling. Set the VIO_Swing register to configure corresponding threshold for 3.3V or 1.8V application.

7.3.9. SPI Interface

The interface to communicate with host is the SPI interface. It supports daisy chain and parallel topology at the same time. The max. speed is up to 16Mhz.

8. Typical Application Diagram



9.Absolute Maximum Ratings

Input Supply Voltage, VCC	-0.3V to 18V
Voltages on CHx, VLEDx, HSx	-0.3V to 40V
Voltages on DAC_FB, VREG5	-0.3V to 5V
Voltages on other pins	-0.3V to 5V
Storage temperature range	-65°C to 150°C
ESD, Charged Device mode (CDM)	600V
ESD, Human body mode (HBM)	2kV
ESD, Machine mode (MM)	200V

10. Electrical Specifications

(V_{IN}=12V, EN=high, LED current=20mA, T_A=25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
System Supply						
Input Supply Voltage	VCC		9	12	16	V
VIN Operation Current	IOP_VIN	VIN=12V, CEN=high VSYNC=120Hz	-	15	-	mA
Undervoltage Lockout Threshold	VUVLO	VIN rising	-	7	7.5	V
	VUVLO_HYS	VIN rising – VIN falling	-	0.5	-	V
Shutdown Current	ISD	EN=0V, VIN=12V	-	-	50	uA
Matrix Switch						
VLED Input Voltage	VLED		3	32	36	V
High-Side ON-Resistance	RHS_ON		-	0.14	-	Ω
Matrix Switch Output Current	IMUX				1.28	A
Matrix Switch Discharge Current	IDIS	Falling time = 150ns		70		mA
Max Matrix Switch Delay	TD_MUX	MUX Delay From VSYNC			1	Frame
Slew Rate		0.2us ~ 3.2us 0.2us/LSB		16		Step
Discharge		10mA ~ 160mA		16	-	Step
Matrix Switch parasitic capacitance				1		nF
IO Voltage Level						
Logic Input Low Level	VIL	VIL < 30% * 3.3V	-	-	1.0	V
Logic Input High Level	VIH	VIH > 70% * 1.8V	1.26	-	-	

Logic Output Low Level	VOL	VOL < 20% * 3.3V VOH > 80% * 1.8V	-	-	0.67	V
Logic Output High Level	VOH		1.44	-		
Pull Down Resistor (EN)	RPD		-	600	-	kΩ
LED Current Regulation						
CHx Leakage Current	ILEAK	VCHx=36V, ICHx=0mA	-	TBD	-	uA
LED Current	ILED		2.5	-	40	mA
I_LED Accuracy			-	+/-2	-	%
LED Current Slew Rate		ICHx = 20mA	100		1600	nS
Minimum CHx Reg	VCH_MIN		0.3		0.6	V
Global Brightness Control	GBC		-	12	-	Bit
Local Brightness Control	LBC		-	11	-	Bit
Channel Parasitic Capacitance				0.5		nF
PWM						
PWM Output Frequency Range	FPWM		40		500	Hz
PWM Resolution	HTPWM			13		bit
PWM Min Pulse Width	TPWM		500			ns
Voltage Feedback						
FB Output Voltage				8		Bit
FB Output Voltage Range			0.2	-	2.5	V
VSYNC						
Frequency Range Of Vsync	FVSYN		40		500	Hz
Multiplier Of VSYN Frequency	KVSYN		1		8	
Duration Time Of Vsync	tVSYN_DUR		40			μs
Internal VCO frequency	FOSC				40	MHz
VCO frequency accuracy				+/-1		%
Fault Detection& Protection						
Output Low Voltage Of INT_B	VINT_L		0		0.5	V
Strong Pull Down Current	IINT_PD		4			mA
Threshold for Open LED Detection	VVD_OLP	Nominal: 50/100/150/200mV	-20%		+20%	mV
Threshold for Short LED Detection	VVD_SLP	Nominal: 3/5/7/9V	-10%		+10%	V
Thermal Shutdown Protection Threshold	TTSP		-	145	-	°C
	TTSP_HYST		-	30	-	°C

11. Serial Peripheral Interface

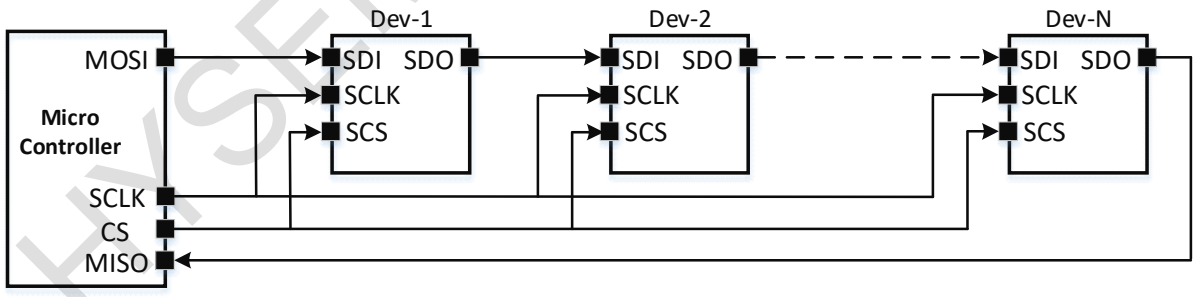
The SPI interface is a synchronous serial interface for address and data transfer at bit rates of up to 16MHz. It is configured in 8-bit data and 11-bit address format designed to interface with a corresponding SPI host. Four pins are used to communicate on the SPI: SCLK (synchronous clock), SCS (chip select, active low), SDI (Write operation), and SDO (Read operation). The corresponding timing specifications are shown below.

Parameter	Symbol	Min	Typ	Max	Unit
SPI Clock Frequency	fSCK	0		16	MHz
SCS Setup Time	tSETUP	10	-	-	ns
SCS Hold Time	tHOLD	10	-	-	ns
SCS Disable Time	tDIS	200	-	-	ns
SDI Setup Time		10	-	-	ns
SDI Hold Time		10	-	-	ns
SCLK Low Time	tL	15	-	-	ns
SCLK High Time	tH	15	-	-	ns
SCLK Rise Time	tR	-	-	10	ns
SCLK Fall Time	tF	-	-	10	ns
Output Vaild from SCLK Low		-	-	10	ns

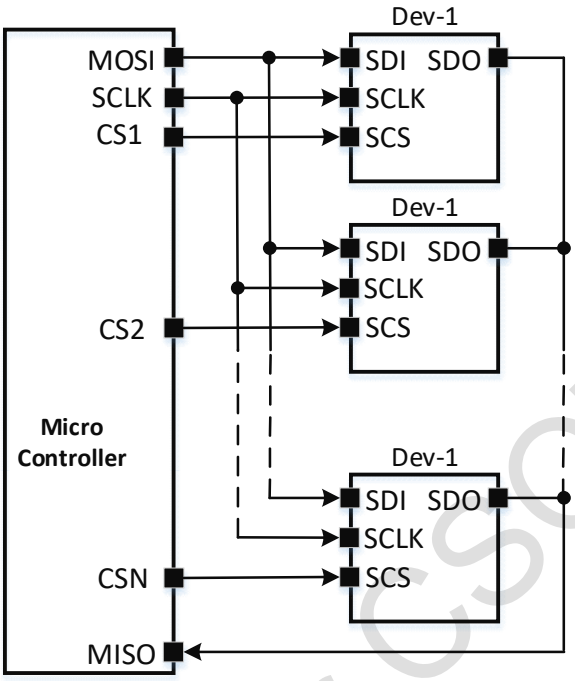
12.1 Topology

There are two topologies available, Daisy Chain & Parallel, for HY88001. The similar structure can be demonstrated below.

12.2 Daisy Chain Structure



12.3 Parallel Structure



12.4 Topology and Device Address

	Daisy Chain Structure	Parallel Structure
Device Addr.	01, 02, 03, …… Nth	01 only
Methodology	Automatically set by the position in the chain	Using individual SCS pin to distinguish device
Connection	SCLK => Share master output clock pin, SCLK SDI => Daisy chain, MOSI -> SDI1 -> SDO1 -> SDI2 ... SCS => Share chip select pin from master, CS SDO => Daisy chain, MOSI -> SDI1 -> SDO1 -> SDI2 … -> MISO	SCLK => Share master output clock pin, SCLK SDI => Share master data output pin, MOSI SCS => Independent chip select pin from master, CSn SDO => Share master input pin, MISO

12.5 Protocol Command

Device ID		
Name	Bit	Description
TA	[7]	1: Configure data to all of device 0: Configure data to single device
SB	[6]	1: Single byte access 0: Multi byte access
DevID	[5:0]	If TA=1 => 0x00 : Configure the same address register with identical data => 0x3F : Configure the same address register with different data If TA = 0 => 0x01 ~ 0x3E : Device ID assignment

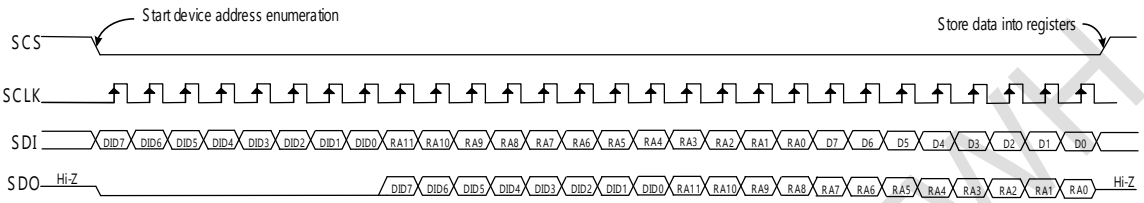
Data Length		
Name	Bit	Description
Block	[7:0]	0x00 ~ 0xFF : Data length for block access

Register Address		
Name	Bit	Description
RW	[11]	1: Read back data from specified register 0: Configure data to specified register
RegAddr	[10:0]	0x000 ~ 0x7FF : Register address

Data		
Name	Bit	Description
Data	[7:0]	0x00 ~ 0xFF : Data content

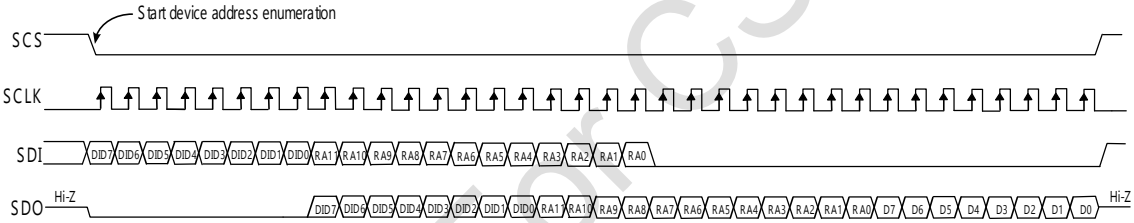
12.6 Generic Write Command Format

Write single data into single device

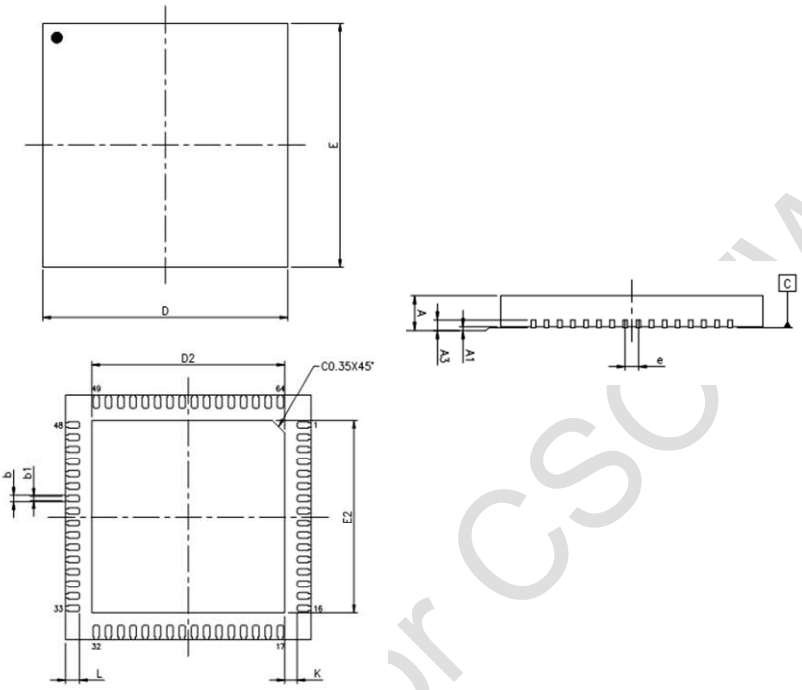


12.7 Generic Read Command Format

Read single data into single device



13 Package Outline Drawing



DIMENSION	MIN (mm)	MAX (mm)
A	0.70	0.80
A1	0.00	0.05
A3	0.203 REF	
b	0.13	0.23
b1	0.07	0.17
D	7.00 BSC	
D2	5.45	5.55
E	7.00 BSC	
E2	5.45	5.55
e	0.35 BSC	
L	0.35	0.45
K	0.20 MIN	

Notes:
1) All dimensions are in millimeters.

14Register Definition

Addr	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
000h	R/W	00h	Zone_dis0[7:0]							
.....										
003h	R/W	00h	Zone_dis0[31:24]							
Zone0 enable/disable control bits. 1b: Enable. 0b: Disable.										

Addr	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
004h	R/W	00h	Zone_dis1[7:0]							
.....										
007h	R/W	00h	Zone_dis1[31:24]							
Zone1 enable/disable control bits. 1b: Enable. 0b: Disable.										

Addr	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
008h	R/W	00h	Zone_dis2[7:0]							
.....										
00Bh	R/W	00h	Zone_dis2[31:24]							
Zone2 enable/disable control bits. 1b: Enable. 0b: Disable.										

Addr	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00Ch	R/W	00h	Zone_dis3[7:0]							
.....										
00Fh	R/W	00h	Zone_dis3[31:24]							
Zone3 enable/disable control bits. 1b: Enable. 0b: Disable.										

Addr	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
010h	R/W	00h	LBC0_x[7:0] (x=0)							
011h	R/W	00h	-	-	-	-	-	LBC0_x[10:8] (x=0)		
.....										
04Eh	R/W	00h	LBC0_x[7:0] (x=31)							
04Fh	R/W	00h	-	-	-	-	-	LBC0_x[10:8] (x=31)		

Local brightness control bits. x: 0~31

Addr	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
050h	R/W	00h	LBC1_x[7:0] (x=0)							
051h	R/W	00h	-	-	-	-	-	LBC1_x[10:8] (x=0)		
.....										
08Eh	R/W	00h	LBC1_x[7:0] (x=31)							
08Fh	R/W	00h	-	-	-	-	-	LBC1_x[10:8] (x=31)		
Local brightness control bits. x: 0~31										

Addr	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
090h	R/W	00h	LBC2_x[7:0] (x=0)							
091h	R/W	00h	-	-	-	-	-	LBC2_x[10:8] (x=0)		
.....										
0CEh	R/W	00h	LBC2_x[7:0] (x=31)							
0CFh	R/W	00h	-	-	-	-	-	LBC2_x[10:8] (x=31)		
Local brightness control bits. x: 0~31										

Addr	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0D0h	R/W	00h	LBC3_x[7:0] (x=0)							
0D1h	R/W	00h	-	-	-	-	-	LBC3_x[10:8] (x=0)		
.....										
10Eh	R/W	00h	LBC3_x[7:0] (x=31)							
10Fh	R/W	00h	-	-	-	-	-	LBC3_x[10:8] (x=31)		
Local brightness control bits. x: 0~31										

Addr	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
110h	R/W	00h	PWM_Bri0_x[7:0] (x=0)							
111h	R/W	00h	-	-	-	PWM_Bri0_x[12:8] (x=0)				
.....										
14Eh	R/W	00h	PWM_Bri0_x[7:0] (x=31)							
14Fh	R/W	00h	-	-	-	PWM_Bri0_x[12:8] (x=31)				
PWM Brightness Control bits. x: 0~31										

Addr	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
150h	R/W	00h	PWM_Bri1_x[7:0] (x=0)							
151h	R/W	00h	-	-	-	PWM_Bri1_x[12:8] (x=0)				
.....										
18Eh	R/W	00h	PWM_Bri1_x[7:0] (x=31)							

18Fh	R/W	00h	-	-	-	PWM_Bri1_x[12:8] (x=31)				
PWM Brightness Control bits. x: 0~31										

Addr	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
190h	R/W	00h	PWM_Bri2_x[7:0] (x=0)							
191h	R/W	00h	-	-	-	PWM_Bri2_x[12:8] (x=0)				
.....										
1CEh	R/W	00h	PWM_Bri2_x[7:0] (x=31)							
1CFh	R/W	00h	-	-	-	PWM_Bri2_x[12:8] (x=31)				
PWM Brightness Control bits. x: 0~31										

Addr	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1D0h	R/W	00h	PWM_Bri3_x[7:0] (x=0)							
1D1h	R/W	00h	-	-	-	PWM_Bri3_x[12:8] (x=0)				
.....										
20Eh	R/W	00h	PWM_Bri3_x[7:0] (x=31)							
20Fh	R/W	00h	-	-	-	PWM_Bri3_x[12:8] (x=31)				
PWM Brightness Control bits. x: 0~31										

Addr	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
210h	R/W	00h	GBC[7:0]							
211h	R/W	00h	-	-	-	-	GBC[11:8]			
Global Brighness Control.										

Addr	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
300h	R/W	00h	-	-	-	-	-	-	-	OpenDet_En
LED Open Detection Enable. 1b: Enable. 0b: Disable.										

Addr	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
310h	R/W	00h	-	-	-	-	-	-	-	ShortDet_En
LED Short Detection Enable. 1b: Enable. 0b: Disable.										

Addr	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
320h	R/W	00h	-	-	-	-	FaultMask[3:0]			
321h	R/W	00h	FaultCLR	-	-	-	-	-	AutoOff_Zone	FaultLch
322h	R/W	00h	FaultRet[7:0]							

FaultMask[3:0]
Fault Mask Time
0000b ~ 0011b => 3 times.
0100b ~ 1111b => 4 ~ 15 times

FaultCLR:
Fault Clear
1: Write only and clear fault status and INT_B, auto clear

AutoOff_Zone:
Auto Turn off Zone
1: Auto turn off abnormal (open/short) zone
0: Turn off abnormal zone by MCU

FaultLch:
Fault Latch
1: Fault status and INT_B keeps till Write FaultCLR
0: Fault status and INT_B will auto clear after Fault retention time expired

FaultRet[7:0]
Fault Retention time
00h : No auto clear feature to status and INT_B
01h~FFh : (1 ~ 255) * Vsync

Addr	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
340h	R/W	03h	-	-	-	-	THDM	HTWM	THD	HTW

THDM:
Thermal Shutdown Fault Mask
1b: Fault recorded and INT_B assertion masked
0b: Fault recorded and INT_B assertion

HTWM:
High Temp. Warning Fault Mask
1b: Fault recorded and INT_B assertion masked
0b: Fault recorded and INT_B assertion

THD:
Thermal Shutdown Enable
1b: Enable
0b: Disable

HTW:
High Temp. Warning Enable
1b: Enable

0b: Disable

Addr	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
341h	R/W	03h	-	-	Short_thres[1:0]		-	-	Open_thres[1:0]	

Short_thres[1:0]:
LED Short detection threshold
11b: 9V
10b: 7V
01b: 5V
00b: 3V

Open_thres[1:0]:
LED Open detection threshold
11b: 0.2V
10b: 0.15V
01b: 0.1V
00b: 0.05V

Addr	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
400h	R/WC	00h	Zone_open0[7:0]							
.....										
403h	R/WC	00h	Zone_open0[31:24]							

LED Open Fault Status
1b: Fault detected
0b: Fault not detected
Writing "1" shall clear the fault bit and set it to 0 again

Addr	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
404h	R/WC	00h	Zone_open1[7:0]							
.....										
407h	R/WC	00h	Zone_open1[31:24]							

LED Open Fault Status
1b: Fault detected
0b: Fault not detected
Writing "1" shall clear the fault bit and set it to 0 again

Addr	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
408h	R/WC	00h	Zone_open2[7:0]							
.....										
40Bh	R/WC	00h	Zone_open2[31:24]							

LED Open Fault Status
1b: Fault detected
0b: Fault not detected

Writing "1" shall clear the fault bit and set it to 0 again

Addr	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
40Ch	R/WC	00h	Zone_open3[7:0]							
.....										
40Fh	R/WC	00h	Zone_open3[31:24]							
LED Open Fault Status 1b: Fault detected 0b: Fault not detected Writing "1" shall clear the fault bit and set it to 0 again										

Addr	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
410h	R/WC	00h	Zone_short0[7:0]							
.....										
413h	R/WC	00h	Zone_short0[31:24]							
LED Short Fault Status 1b: Fault detected and the corresponding LED driver will be disabled 0b: Fault not detected Writing "1" shall clear the fault bit and set it to 0 again										

Addr	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
414h	R/WC	00h	Zone_short1[7:0]							
.....										
417h	R/WC	00h	Zone_short1[31:24]							
LED Short Fault Status 1b: Fault detected and the corresponding LED driver will be disabled 0b: Fault not detected Writing "1" shall clear the fault bit and set it to 0 again										

Addr	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
418h	R/WC	00h	Zone_short2[7:0]							
.....										
41Bh	R/WC	00h	Zone_short2[31:24]							
LED Short Fault Status 1b: Fault detected and the corresponding LED driver will be disabled 0b: Fault not detected Writing "1" shall clear the fault bit and set it to 0 again										

Addr	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
41Ch	R/WC	00h	Zone_short3[7:0]							
.....										
41Fh	R/WC	00h	Zone_short3[31:24]							

LED Short Fault Status
1b: Fault detected and the corresponding LED driver will be disabled
0b: Fault not detected
Writing "1" shall clear the fault bit and set it to 0 again

Addr	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
420h	R	00h	THDF	HTWF	-	-	-	-	-	-

THDF:
Thermal Shutdown Fault:
1b: Fault detected
0b: Fault not detected

HTWF:
1b: OTP load finished

High Temp. Fault
1b: Fault detected
0b: Fault not detected

Addr	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
477h	R	31h	PartNo[15:8]							
478h	R	02h	PartNo[7:0]							
479h	R	AAh	VerID_Body[3:0]				VerID_Code[3:0]			

PartNo[15:0]:
Part No. = 0x3102

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